A Simple I/O Buffer Circuit for Mixed Voltage Applications

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Abstract: - A very simple circuit design of a bidirectional input/output(I/O) buffer is proposed for mixed voltage interface applications. By a floating N-well circuit technique two series PMOS transistors are used as an active pull-up driver. Such a structure provides a simple circuit that requires only a single terminal pad, a single power supply, and is free of DC leakage current. Mixed voltage interface applications such as 3.3V/5V are demonstrated.

Key-Words: - I/O buffer, Mixed voltage, Interface, Floating N-well, Single pad, Single terminal, DC leakage

1 Introduction

As the process technology advances the standard power supply voltage VDD is reduced from 5V to 3.3V for half-micron VLSI's. This translation in DC power supply voltage from 5V to 3.3V will approximately save power consumption by forty percent. Due to this reason, power reduction in integrated circuits (IC's) has become a priority. However, during the long anticipated transition period to completely convert 5V to 3.3V, both 5V and 3.3V digital IC's will be used in system and board designs. For example, a system memory may operate with a 3.3V power supply but its monitor may require 5V. Thus, a 3.3V/5V compatible bidirectional buffer is desired. For such interface situation between chips, many problems will arise. One of the major problems is that a 5V output buffer may drive a 3.3V bidirectional bus driver or both 5V and 3.3V output buffers share a common bus.

As shown in Fig. 1 is a conventional 3.3V input/output (bidirectional) circuit. Depending on the value of the Output Enable (Enable) control signal, the direction of data transmissions is determined. For example, when the Enable signal has a value of logic "0", this buffer acts as an input buffer, and when the Enable signal has a value of logic "1", this buffer acts as an output buffer. During the input phase, the driver transistors P1 and N1 are both off since the voltage levels at their respective gates are VDD and VSS, respectively. However, when a 5V input signal is applied to the pad two conducting paths to the 3.3V power supply will appear.

First, the parasitic diffusion diode of the PMOS P1 to the N-well will become forward biased. And second, the PMOS P1 itself will conduct current from pad OUT to the 3.3V power source VDD since its gate-to-drain voltage is larger than its threshold voltage (in absolute value). Therefore, hazards, such as functional failure, may occur not only due to the loading value of the input signal but also due to the reverse current in the power supply.
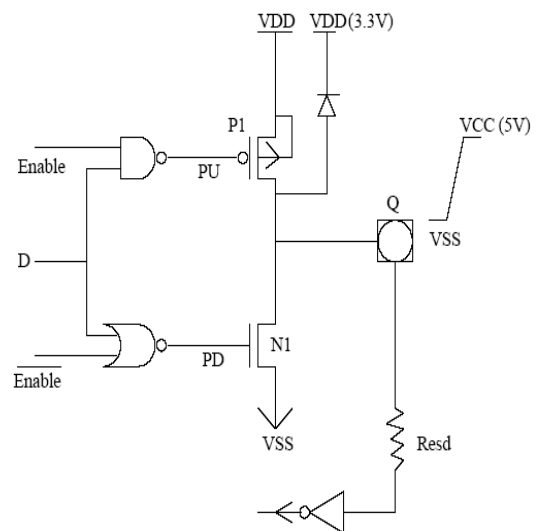

Fig. 1 Conventional 3.3V I/O buffer driven by a 5V signal

2 Prior Art

Many prior arts which deal with the 3.3V/5V interface problem have been disclosed [1]--[8]. In the literature, a pseudo N-well technique is presented [1]. To eliminate the first conducting current, the P1's N-well has to be tied to the 5V power supply (external and higher power). However,

the second conducting current path also exits. Besides, this arrangement results in two main disadvantages including (1)dual powers in the same chip (3.3V/5V); and (2)additional bonding pad (for connecting P1's N-well to the external power). In addition, the PMOS driver transistor P1 still has DC leakage current when the applied external signal is 5V.

As in [2], this prior art eliminates all possible conducting currents mentioned above. However, three or two power supply voltages are required in the same chip. Besides, level-shifting circuits are also required for interface purpose. This inevitably leads to much more circuit and layout complexity. Recently, a 3/5 V compatible I/O buffer is proposed [3], as shown in Fig. 2. In this circuit, advantages of single power, no DC leakage current of P1 and no additional bonding pad are provided by a "floating N-well" circuit technique. That is, a lot of PMOS transistors are laid out in a floating N-well. However, as compared to the conventional bidirectional buffer, this prior art circuit needs 12 additional MOS transistors and therefore it is of high cost in terms of silicon area.

Fig. 3 shows a proposed 3.3V/5V compatible CMOS bidirectional buffer. In the following, the circuit structure is described first:

(1) pull-up driver: P1 and P2 (associated with parasitic diodes D1 and D2);
(2) pull-down driver: N1 only;
(3) operation control cicuit: N2, P3;
(4) tri-state control logic: NAND and NOR gates;
(5) input buffer with electro-static discharge protection resistor Resd.

The main feature of this circuit is "series-connected PMOS P1 and P2 which are arranged in a floating N-well". Due to the N-well connection, two parasitic diodes D1(P1's source to N-well) and D2(P2's drain to N-well) are associated with their cathode to cathode. Besides, an operation control circuit which consists of N2 and P3 is also provided. Note that P3 can be laid-out with its N-well tied to node OUT or in the floating N-well, too. The operation control circuit receives the control signal "Enable"(output enable) as an input and generates corresponding activate/deactivate signals to P1.
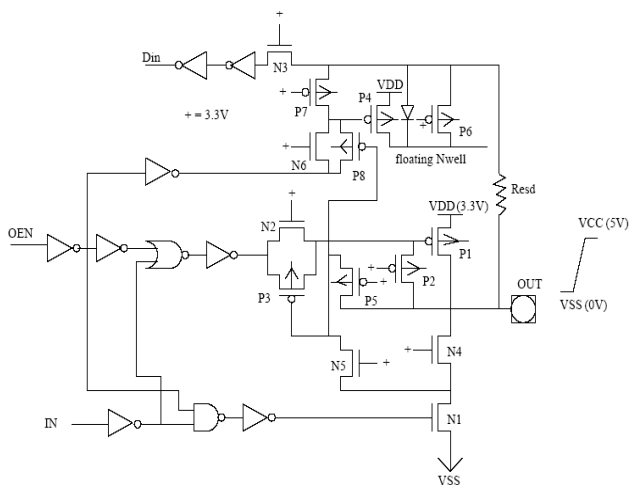

Fig. 2 3.3V/5V compatible I/O buffer driven by a 5V signal

In other references [4]--[8] process option or additional interface IC is provided to cope with the mixed voltage interface problem. However, more process steps or IC components are needed and so lead to very expensive cost. So, in this paper, a simple circuit structure is proposed to overcome all mentioned-above disadvantages
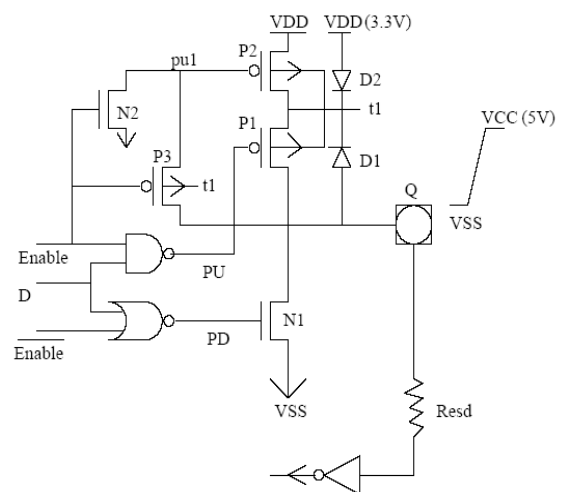
3 Proposed Circuit

Fig. 3 Proposed simple circuit design

In the following, circuit operations are described. First, consider Enable="1", that is, the bidirectional buffer is for output use. In this condition, P3 is off while N2 is turned on to make the voltage level of node pu1 "0". Since a low voltage is applied to P1's gate, it is turned on to pull the voltage potential of the floating N-well(t1) up to 3.3V. Therefore, the floating N-well is biased to 3.3V when the buffer outputs data. Since Enable="1", NAND gate and NOR gate are logically inverters only.

When the output data IN is "1", both signals PU and PD are "0". In this condition, N1 is off while P1 and P2 are on to pull the output terminal OUT up to 3.3V. On the contrary, when the output data IN is "0", both signals PU and PD are "1". In this condition, P2 is off while N1 is on to pull the output terminal OUT down to 0V.

Then consider IN makes a transition from "1" to "0". As the signal IN decreases, the output of the NOR gate increases, so N1 is turned on. At the same time, the output of the NAND gate also increases, so P2 begins to cut off. Since the pull-down driver N1 is on, so the output OUT is finally discharged all the way to VSS.

Now consider IN makes a transition from "0" to "1". As the signal IN increases, the output of the NOR gate decreases, so N1 is turned off. At the same time, the output of the NAND gate also decreases, so P2 begins to conduct. Since the pull-up driver P1, P2 is on, so the output OUT is finally charged all the way to VDD. However, this transient condition needs to be carefully checked.

As below, three design principles are given for proper circuit operation and much enhanced latchup immunity. When the output terminal OUT transitions from 'L' to 'H' two charge paths are provided. The first path is through the series P1 and P2. The second path results from the series D1 and P2. The second path is actually not desired since the parasitic D1 becomes forward biased. In fact, even D1 turns on the initial turn-on current is not infinite because P2 is initially a large resistance. Consider the case of D1 that it is forward biased the latchup problem may potentially arise. To cope with this problem three design principles are suggested in the following:

(1) P1's strength stronger than P2's is preferred. If the P1's strength is stronger than P2's (X3 or X4 times), the voltage potential of the floating N-well t1 can be kept close to 3.3V since the charge flowing out through P2 is less than the charge supplied from VDD through P1. As the accumulated charge is not removed to a much degree, the diode D1 is even kept in the reversed-biased state.

(2) Layout arrangement: Separate the PMOS and NMOS devices by the large bonding pad. If the PMOS and NMOS devices are laid-out in the opposite sides of the bonding pad, the potential latchup resulting from P-N-P-N path may never arise.

(3) Double guard ring structure: Since this circuit is an I/O cell, the traditional layout technique called double guard ring structure should be applied. For CMOS IC's a double guard ring structure is actually the most effective layout technique to make latchup free.

Next, consider Enable="0", that is, the bidirectional buffer is for input use. In this case, N2 is off while P3 is on. Both control signals are now PU=3.3V and PD=0V, respectively. When the input signal applied to the output terminal OUT is "0"(0V), this low voltage can be sustained well. When the input signal applied to the output terminal OUT is "1"(5V), this high voltage can be sustained well, too. Under this condition, node pu1 is pulled up to 5V since P3 is on. P2 is also turned on because its gate-to-drain voltage is -1.7V(3.3V-5V=-1.7V). Therefore, node t1 is pulled up to 5V. As the gate and drain of P1 are both 5V, P1 remains off. Besides, both D1 and D2 are reverse-biased. Therefore, the bidirectional buffer has no DC leakage current for both output and input operations.

4 Results and Discussions

Fig. 4 and Fig. 5 are simulation results according to Fig. 3 circuit (input: IN and output: OUT) for an input of 50MHz without and with loading 20pF, respectively. These simulation results are based on 0.35μm process parameters. In this example 4 times of P1's strength to P2's is used. For simulation purpose, this proposed 3.3V/5V compatible I/O buffer is driven by a conventional 5V tri-state output buffer circuit. Judging from these results, proper circuit operations are acquired. Most of all, the parasitic diode D1 even never becomes forward-biased as illustrated in Fig. 5. This consequence is solely due to the design principle with the mechanism mentioned before.
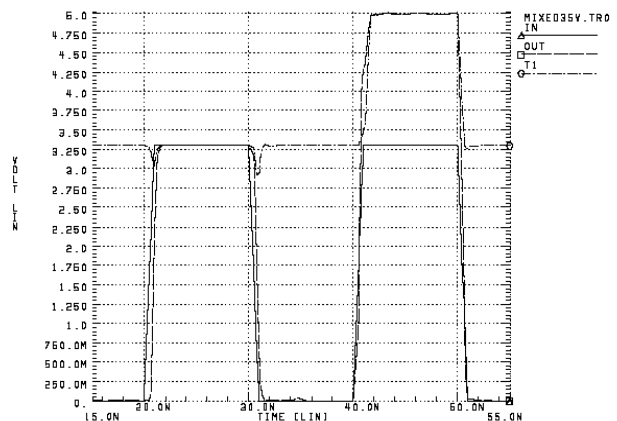

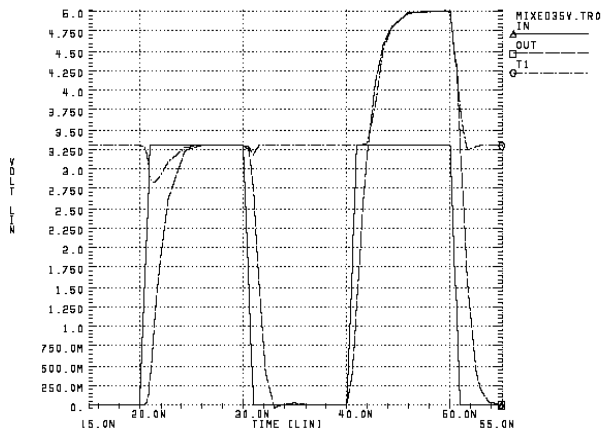Fig. 4 Simulation results I(50MHz input, no load)

Fig. 5 Simulation results II(50MHz input, with load)

As for Fig. 6, the corresponding power/ground current waveforms to Fig. 5 are shown. Note that there is no DC leakage current in steady state operations. Furthermore, 2.5V/3.3V interface applications are also examined as shown in Fig. 7. The whole circuit functions show very satisfactory results in this low voltage interface condition.
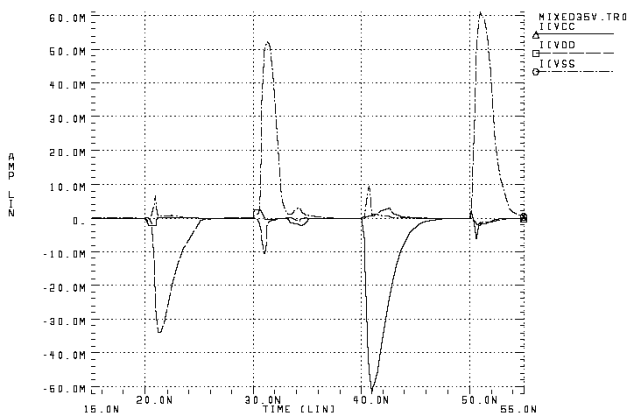

Fig. 6 Corresponding power/ground current waveforms to Fig. 5

In fact, as compared to the prior arts, this proposed circuit is the succinctest design in the literature since only 3 additional MOS transistors are needed. In addition to its simplicity, this proposed circuit also provides advantages of only single power, no DC leakage current and no additional bonding pad. Therefore, this proposed design is a perfect solution to the mixed voltage interface problem and has the lowest cost in terms of circuit implementation.
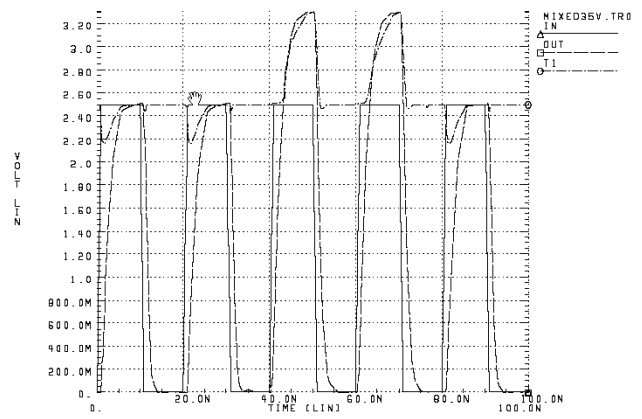

Fig. 7 Low voltage 2.5V/3.3V interface application

5 Conclusion

In this paper, a bidirectional buffer has been demonstrated for interface applications in a mixed voltage system. By a floating N-well circuit technique a very simple circuit design in the literature is achieved. Based on circuit simulation results the validity of the proposed circuit is confirmed. Therefore, this proposed circuit is very suitable for mixed voltage interface applications such as deep submicron technology IC's with least silicon cost.

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